REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claims 11, 12 and 13 and added new Claim 18. Applicants have also amended the specification.

Specifically, applicants have amended Claim 11 to clearly and positively recite that at least one NFET and at least one PFET each have a device channel that is parallel to the semiconducting substrate surface. Support for this amendment is found throughout applicants' specification. See, for example, paragraph [0032] and FIGS. 4- 5(F). Referring to FIG. 5(F) of the instant application, applicants clearly disclose that the source and drain region 58 are formed within the substrate, wherein the device channel separating the source and drain regions 58 is parallel to the substrate surface.

Applicants have also amended Claim 11 to state that the semiconducting substrate is a Group IV semiconducting material to more clearly and positively recite an aspect of the present invention. Applicants claimed invention relates to increased carrier speed for p-type and n-type semiconducting devices on the same semiconducting wafer by positioning the specific devices on optimized crystalline orientation surfaces. Referring to paragraphs [0028] and [0029] of the instant specification, applicants have determined optimum surface orientations and current flow for nFET and pFET devices formed on substrates comprising Group IV (Group IV of the Periodic Table of Elements) semiconducting materials. Dependent Claims 12 and 13 have been amended to be consistent with amended base Claim 11. Therefore, since the amendments to Claims 11-13 are not new matter, applicants respectfully request that the amendments to Claims 11-13 be entered.

Applicants have also added new Claim 18. Newly added Claim 18 recites an

integrated semiconductor structure that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate, wherein the at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, the <110> direction is perpendicular to the <100> direction, wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.

Applicants note that newly added Claim 18 includes the limitations of original Claims 11 and 14. Referring to Page 2 of the present Office Action, the Examiner admits that dependent Claim 14 is allowable subject matter if rewritten in independent form including all of the limitations of the base Claim 11. Therefore, since newly added Claim 18 recites the limitations of original Claim 11 and includes the limitations of original Claim 14, applicants request that newly added Claim 18 be entered and be allowed. Applicants have also amended paragraph [0030] of the specification to remove Group III/V materials from the list of Group IV semiconducting materials.

In the Office Action, Claims 11, 13 and 17 stand rejected under 35 U.S.C. §103(a), as allegedly unpatentable over the English translation of Japanese Patent Abstract JP 01076755 to Yasukawa ("Yasukawa") in view of U.S. Patent No. 6,483,171 to Forbes, et al. ("Forbes, et al.") in further view of the English translation of Japanese Patent Abstract JP 411354394 to Yasukawa ("Yasukawa"). Claims 14-16 are allowable subject matter but stand objected to as being dependent upon a rejected base claim. Applicants traverse the aforementioned rejections and submit the following.

Applicants respectfully submit that the applied references do not render applicants' invention unpatentable, since the applied references fails to teach or suggest applicants' claimed semiconducting structure, as recited in amended Claim 11. Applicants' claimed

semiconducting structure comprises a semiconductor substrate comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and at least one PFET and at least one NFET located on the semiconductor substrate, *the at least one PFET and the at least one NFET each having a device channel parallel to a surface of the semiconducting substrate,* wherein at least one PFET has a current flow in a <110> direction and at least one NFET has a current flow in a <100> direction, the <110> direction is perpendicular to the <100> direction. "To establish a prima facie case of obviousness of a claimed invention all the claimed limitations must be taught or suggested by the prior art". *In re Wilson,* 424 F.2d 1382, 1385, 165 USPQ 44, 496 (CCPA 1970).

Yasukawa does not render applicants' claimed semiconductor structure unpatentable, since Yasukawa does not teach or suggest a semiconducting structure including *at least one NFET device and at least one PFET device each having a device channel parallel to a surface of the semiconducting substrate, wherein the at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, the <110> direction being perpendicular to the <100> direction*, as recited in amended Claim 11. Referring to Page 2 of the Office Action, the Examiner admits that, "Yasukawa fails to disclose an NFET structure in which current flows in a <100> direction and the notch pointing in a <001> direction of current flow." Therefore, since Yasukawa fail to teach or suggest an NFET structure in which current flows in a <100> direction, Yasukawa fail to teach or suggest an NFET device in which current flows in a <100> direction and has a device channel parallel to the substrate surface, wherein current flow through the NFET device is perpendicular to current flow through a PFET device, as recited in amended Claim 11. Yasukawa also fails to teach or suggest a Group IV semiconducting material that has a (100) surface orientation and a notch pointing in a <001> direction of current flow.

Forbes, et al. fail to fulfill the deficiencies of the primary reference, Yasukawa, since Forbes, et al. also fail to teach or suggest a semiconducting structure comprising *at least one*

NFET device and at least one PFET device each having a device channel parallel to the surface of a semiconducting substrate, wherein at least one PFET has a current flow in a <110> direction and at least one NFET has a current flow in a <100> direction, the <110> direction being perpendicular to the <100> direction, as recited in amended Claim 11. Forbes, et al. disclose forming *vertical transistors* on a (100) semiconducting surface, in which the direction of current through the vertical transistor is in a <110> direction. The vertical transistors disclosed in Forbes, et al. have source regions, device channel regions and drain regions stacked atop a semiconducting substrate. The device channel of the vertical transistors disclosed in Forbes, et al. is in a direction perpendicular to the substrate surface. Therefore, since the device channel of the devices disclosed in Forbes, et al. is perpendicular to the semiconducting surface, Forbes, et al. fail to teach or suggest a semiconducting structure comprising at least one NFET device having a device channel parallel to the substrate surface, wherein current flow through the at least one NFET device is perpendicular to current flow through at least one PFET device, as recited in amended Claim 11. Forbes, et al. also fail to teach or suggest a Group IV semiconducting substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow.

Applicants further submit that the vertical devices disclosed in Forbes, et al. can not be combined with the primary reference, Yasukawa, to provide applicants' claimed structure. Forbes, et al. cannot be combined with Yasukawa to provide applicants' claimed structure, because Forbes, et al. disclose vertical transistors and Yasukawa disclose planar transistors. Vertical transistors can not be orientated to planar transistors to provide a device having at least one PFET and at least one NFET each having a device channel parallel to the surface of a semiconducting substrate, wherein the at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, the <110> direction being perpendicular to the <100> direction, as recited in amended Claim 11. Therefore, the combination of Forbes, et al. and Yasukawa does not teach or suggest each and every aspect of applicants' claimed invention.

Sawada also fails to fulfill the deficiencies of the prior art, since Sawada also fails to teach or suggest applicants' claimed structure, as recited in amended Claim 11. Sawada discloses a means for reducing the occurrence of slip defects in GaAs substrates. Sawada do not disclose forming NFET and PFET devices and therefore fail to teach or suggest providing a semiconducting structure comprising at least one NFET device and at least one PFET device each having a device channel parallel to a surface of the semiconducting substrate, wherein the at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, in which the <110> direction is perpendicular to the <100> direction, as recited in amended Claim 11

Applicants note that Sawada is far removed from applicants' claimed structure. Applicants observe that Sawada is relied upon for providing a notch in a GaAs substrate pointing in the <100> direction. Applicants submit that Sawada discloses GaAs substrates, a Group III/V substrate material, and applicants' claimed invention is directed to crystalline orientation based device improvements in semiconducting substrates from Group IV of the Periodic Table of Elements, such as Si. The directional dependencies that enhance device performance in Group IV semiconducting substrates are entirely different from Group III/V semiconducting substrates. Therefore, in addition to failing to teach or suggest an NFET device in which current flows in a <100> direction and has a device channel parallel to the substrate surface and perpendicular to the device channel of at least one PFET device, Sawada also fails to teach or suggest a semiconductor substrate comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow, as recited in amended Claim 11.

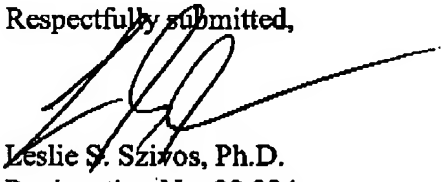
The §103 rejections also fail because there is no motivation in the applied references, which suggest modifying the disclosed structures provide a semiconductor substrate *comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow*; and at least one PFET and at least one NFET located on the semiconductor substrate, *said at least one PFET and said at least one*

NFET each having a device channel parallel to a surface of said semiconducting substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction, as recited in amended Claim 11. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Vaeck*, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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